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09/494,567	01/31/2000	Martin Vorbach	2885/29	3627

26646 7590 07/24/2003

KENYON & KENYON  
ONE BROADWAY  
NEW YORK, NY 10004

EXAMINER

MEONSKE, TONIA L

ART UNIT	PAPER NUMBER
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2183

DATE MAILED: 07/24/2003

6

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/494,567

Applicant(s)

VORBACH ET AL.

Examiner

Tonia L Meonske

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 31 January 2000.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-11 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-11 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 31 January 2000 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.  
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☒ Certified copies of the priority documents have been received in Application No. 08/946,998.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 3,5.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other:

## **DETAILED ACTION**

### ***Priority***

1. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in parent Application No. 08,946,998, filed on October 8, 1997.

### ***Drawings***

2. This application lacks formal drawings. The informal drawings filed in this application are acceptable for examination purposes. When the application is allowed, applicant will be required to submit new formal drawings.

### ***Information Disclosure Statement***

3. The information disclosure statement filed January 10, 2001 fails to comply with 37 CFR 1.98(a)(3) because it does not include a concise explanation of the relevance, as it is presently understood by the individual designated in 37 CFR 1.56(c) most knowledgeable about the content of the information, of each patent listed that is not in the English language. It has been placed in the application file, but the information referred to therein with respect to the following citations have not been considered:

i.	19651075	October 6, 1998	Germany
ii.	19654595	July 2, 1998	Germany
iii.	19654846	July 9, 1998	Germany
iv.	4416881	May 13, 1993	Germany
v.	19704728	August 13, 1998	Germany.

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4. The information disclosure statement filed January 10, 2001 fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each U.S. and foreign patent; each publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. It has been placed in the application file, but the information referred to therein with respect to the following citations has not been considered:

- a. US Patent 5,128,559
- b. US Patent 5,142,469
- c. US Patent 5,943,242
- d. European Patent 726532

5. The information disclosure statement filed January 10, 2001 fails to comply with 37 CFR 1.98(b), which requires that each item of information in an IDS be identified properly. U.S. Patents must be properly identified by the inventor, patent number, and issue date. *See MPEP 609 III. A.* The IDS has been placed in the application file, but the information referred to therein with respect to the following citations has not been considered, as each item of information is not identified properly (i.e. improper date and/or improper inventor name):

- a. US Patent 4,489,857;
- b. US Patent 4,591,979;
- c. US Patent 5,043,978;
- d. US Patent 5,115,510;
- e. US Patent 5,440,538;
- f. US Patent 5,590,348;
- g. US Patent 5,596,742;

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- h. US Patent 5,617,547;
- i. US Patent 5,634,131;
- j. US Patent 5,652,894;
- k. US Patent 5,655,124;
- l. US Patent 5,713,037;
- m. US Patent 5,717,943;
- n. US Patent 5,742,180;
- o. US Patent 5,754,871;
- p. US Patent 5,761,484;
- q. US Patent 5,778,439;
- r. US Patent 5,828,858;
- s. US Patent 5,838,165;
- t. US Patent 5,867,691;
- u. US Patent 5,892,961;
- v. US Patent 5,915,123;
- w. US Patent 5,927,423;
- x. US Patent 5,936,424;
- y. US Patent 5,956,518;
- z. US Patent 6,014,509;
- aa. US Patent 6,052,773;
- bb. US Patent 6,054,873;
- cc. US Patent 6,127,908;

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- dd. US Patent 4,761,755;
- ee. US Patent 5,583,450; and
- ff. European Patent 748 051 A2.

6. Furthermore, even though the above-mentioned references have not been officially considered and made of record, Examiner has looked at the references and determined that no rejection could be applied with the above-mentioned references.

### ***Claim Objections***

7. Claims 1-11 are objected to as being in an improper format. All claims should be a sentence whereby the claims begin with a capital letter and end with a period. See MPEP 608.01(m). There should be no more than one period per claim otherwise it is unclear where the claim ends. The body of claim 1 contains 9 periods. Please delete the following limitations from claim 1: "1.", "2.", "3.", "4.", "5.", "6.", "7", and "8.". Furthermore, before:

- i. claim 1, please change "1." to "1.";
- ii. claim 2, please change "2." to "2.";
- ii. claim 3, please change "3." to "3.";
- iv. claim 4, please change "4." to "4.";
- v. claim 5, please change "5." to "5.";
- vi. claim 6, please change "6." to "6.";
- vii. claim 7, please change "7." to "7.";
- viii. claim 8, please change "8." to "8.";
- ix. claim 9, please change "9." to "9.";
- x. claim 10, please change "10." to "10."; and

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xi. claim 11, please change “11:” to “11.”.

8. Claim 1 is objected to because of the following informalities:

i. In line 4, the acronym “PLU” is introduced into the claim. However, in claim 1 Applicant has failed to spell out the words the acronym represents. Please include the words along with the acronym the first time the acronym is introduced into the claim.

ii. In lines 10-11, 15, 21, 23, and 25, the limitation “the configuration data” lacks an antecedent basis. To correct this, in line 7, please insert the limitation “configuration” before the limitation “data”.

iii. In line 7 please insert the limitation “address of an” before the limitation “can calculate an”.

iv. In line 8, please replace the limitation “on the basis of the” with the limitation --based on a --.

v. In line 10 please replace the limitation “the address, which was calculated,” with the limitation --the calculated address--.

vi. In line 16, please replace the limitation “element(s)” with the limitation --cell(s)--.

vii. In line 18, please replace the limitation “on the basis of” with --based on--.

viii. In line 19, please delete the limitation “which”.

ix. In line 19, please replace the limitation “each” with the limitation --a--

x. In line 20, please insert the limitation “of each cell” before the limitation “reloading”.

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- xi. In line 22, please replace the limitation “or” with the limitation --and--.
- xii. In line 24, please insert the limitation --entry corresponding to the-- before the limitation “calculated”.
- xiii. In line 24, please insert the limitation --address in the-- before the limitation “jump table”.
- xiv. In line 24, please delete the limitation “entry”.
- xv. In line 25, please delete the limitation “stored at the address read out”.
- xvi. In line 26, please insert the limitation --either-- before the limitation “loaded”.
- xvii. In line 26, please insert the limitation --the-- before the limitation “cells”.
- xviii. In line 27, please replace the limitation “reprogrammed” with the limitation --reconfigured--.
- xix. In line 28, please insert the limitation --one or more-- before the limitation “PLU”.
- xx. In line 28, please replace the limitation “PLU” with --PLU’s--.
- xxi. In line 28, please replace the limitation “returns” with --return--.
- xxii. In line 28, please replace the limitation “it” with --they--.

gg. Appropriate correction is required.

9. Claim 1 is further objected to for the following reasons. Claim 1 contains the limitation “a FIFO memory area which is run through before each reloading”. The limitation “run through” is obscure and unclear. It could at least have one of the following meanings: 1) Always transmit the configuration data through the FIFO when transferring the data to the PLU’s, 2) Literally run



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through the FIFO, or 3) Check to see if the FIFO is empty. For purposes of examination the third definition is assumed. Appropriate correction is required.

10. Claim 5 is objected to because of the following informalities:

- i. In line 2, please change “the” to --a--.
- ii. In line 3, please change “the” to --a--.
- iii. In line 4, please change “are” to --is--.

Appropriate correction is required.

11. Claim 6 is objected to because of the following informalities:

- i. In line 2, please change “the” to --an--.
- ii. In line 3, please change “the” to --a--.
- iii. In line 4, please change “are” to --is--.

Appropriate correction is required.

12. Claim 7 is objected to because of the following informalities:

- i. In line 3, please change each occurrence of the limitation “the” to --a--.
- ii. In line 4, please change “are” to --is--.

Appropriate correction is required.

13. Claim 9 is objected to because of the following informalities:

- i. In line 2, please change “the” to --an--.

Appropriate correction is required.

14. Claim 11 is objected to because of the following informalities:

- i. In line 4, please change “the” to --a--.

Appropriate correction is required.

***Claim Rejections - 35 USC § 103***

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

16. Claims 1-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Casselman, US Patent 5,802,290, in view of Rodgers et al., US Patent 5,889,982 and Schrofer, US Patent 4,682,284.

17. Referring to claim 1 Casselman has taught the method of run-time reconfiguration of programmable units with a two- or multi-dimensional cell architecture (e.g., FPGAs, DPGAs, DFPs, etc.) (Casselman, abstract, Figure 3), characterized in that

a. there are one or more PLUS which respond to signals, regardless of type (Casselman, Figure 5, column 3, lines 14-21, column 4, lines 35-46, There is no indication that the PLU's selectively respond to signals so therefore the PLU's respond to signal regardless of type.) and can recognize and process special PLU commands within a configuration program consisting of data and commands (casselman, Figure 17, elements, elements 700 and 702, column 16, line 49-column 17, line 10, The configuration program is the program running on the mother FPGA that reconfigures the Daughter FPGA.),

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- b. there are one or more configuration memory areas into which one or more configuration programs are loaded (Casselman, Figure 4, The memory area where the configuration bit files that are produced by the mother FPGA are stored.),
  - c. the configuration data is transferred to the cell (Casselman, Figure 17, element 710, 712, 714),
  - d. the configuration data stored at the address read out is loaded into cells (Casselman, Figure 17, element 710, 712, 714)
  - e. the PLU returns to a state in which it can wait for events and respond to them (This is normally how computer systems operate. Casselman, Column 3, lines 4-21, The FPGA's wait to be reconfigured all the time.).
18. Casselman has not specifically taught that the PLU can calculate an entry in a jump table on the basis of the source of an event, there are one or more jump tables for discovering the address, which was calculated, of the configuration data to be loaded, an event occurs and an address in a jump table is calculated on the basis of the source of the event, and the calculated jump table entry is read out. Casselman has taught that rapidly transitioning between operating modes, or configuration modes, is desirable (Column 3, lines 4-20).
19. Rodgers has taught an efficient method for transitioning between operating modes. Rodgers has taught
- a. calculating an entry in a jump table on the basis of the source of an event (Rodgers et al., column 16, line 50-column 17, line 3, The exception vector is the address for the entry in the event ROM.),

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- b. there are one or more jump tables for discovering the address, which was calculated, of the configuration data to be loaded (Rodgers et al., column 16, line 50-column 17, line 3, The event ROM 133 contains 14 bit pointers to the microcode event handlers.),
  - c. an event occurs and an address in a jump table is calculated on the basis of the source of the event (Rodgers et al., column 16, line 50-column 17, line 3, The exception vector is the address for the entry in the event ROM. The address is calculated based on the source of an event, or type of exception.),
  - d. the calculated jump table entry is read out (Rodgers et al., Abstract, column 16, line 50-column 17, line 3, In order to invoke the microcode event handler the entry in the table must be read out.)
20. in order to service mode switching events efficiently (Rodgers et al., column 17, lines 29-41).
21. It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the efficient method of transitioning between operating modes using look-up tables, as taught by Rodgers et al., into the invention of Casselman, for the desirable purpose of rapidly transitioning between varying configuration modes of the PLU's.
22. Casselman has not specifically taught
- a. there are one or more FIFO memory areas to which configuration data that could not be sent to the element(s) to be configured is copied, a FIFO memory area is run through before each reloading, if the cell cannot be reloaded, the configuration data is

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copied closer to the beginning of the FIFO memory area, and the configuration data is copied to the FIFO memory area if the cell cannot be reprogrammed.

23. However, Schrofer has taught

a. there are one or more FIFO memory areas to which configuration data that could not be sent to the element(s) to be configured is copied (Schrofer, Abstract Figure 3, element 301),

b. a FIFO memory area is run through before each reloading (Schrofer, Column 2, lines 29-34), and if a request cannot be transferred to the executing apparatus, then the configuration data is copied closer to the beginning of the FIFO memory area (Schrofer, Abstract, Columns 2 and 3, Column 2, lines 29-34, the request is copied to the Queue when the executing apparatus is not ready to accept requests.), and the configuration data is copied to the FIFO memory area if the cell cannot be reprogrammed (Schrofer, Abstract, Columns 2 and 3, Column 2, lines 29-34, If the executing apparatus is not ready to receive requests, then the request is stored in the queue for later processing.), for the desirable purpose of being able to queue up requests to the executing apparatus even when the executing apparatus is not ready itself to accept requests (Column 5, lines 40-50). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the FIFO memory area, as taught by Schrofer, into the invention of Casselman, for the desirable purpose of being able to queue up configuration data to the PLU's even when the PLU's cannot currently be reconfigured (Column 5, lines 40-50) so that the system may continue processing data even when the PLU's are not ready to be reconfigured.

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24. Referring to claim 2, Casselman in combination with Rodgers et al. and Schrofer have taught the method according to Claim 1, as described above, and characterized in that the configuration memory stores one or more configurations containing one or more complete configurations for one or more units (Column 12, lines 18-39, When an FPGA is reconfigured to implement a user selected algorithm, the configuration memory stores a complete configuration bit file.).

25. Referring to claim 3, Casselman in combination with Rodgers et al. and Schrofer have taught the method according to Claim 1, as described above, and characterized in that the configuration memory stores one or more subconfigurations representing only part of a complete configuration of one or more units (Column 12, lines 18-39, When an FPGA is reconfigured to implement only a portion of a user selected algorithm, the configuration memory stores a subconfiguration representing only a part of a complete configuration of the units.).

26. Referring to claim 4, Casselman in combination with Rodgers et al. and Schrofer have taught the method according to Claim 1, as described above, and characterized in that the PLU contains a start configuration register which points at a start configuration that puts the units in a valid state (Rodgers et al., column 16, line 50-column 17, line 3, The entry read out of the table points at a start configuration that puts the units in a valid state.).

27. Referring to claim 5, Casselman in combination with Rodgers et al. and Schrofer have taught the method according to Claim 1, as described above, and characterized in that the PLU contains a FIFO start register which points at the start of the specific memory area to which configuration data is copied (Schrofer, Column 9, lines 5-30).

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28. Referring to claim 6, Casselman in combination with Rodgers et al. and Schrofer have taught the method according to Claim 1, as described above, and characterized in that the PLU contains a FIFO end register which points at the end of the specific memory area to which configuration data are copied (Schrofer, Column 9, lines 30-57, Column 12, lines 57-63).

29. Referring to claim 7, Casselman in combination with Rodgers et al. and Schrofer have taught the method according to Claim 1, characterized in that the PLU contains a FIFO free entry register which points at the free entry of the specific memory area to which configuration data are copied and which is closest to the start of this memory area (Schrofer, Column 9, lines 30-57).

30. Referring to claim 8, Casselman in combination with Rodgers et al. and Schrofer have taught the Method according to Claim 1, characterized in that the PLU contains a program counter register which points at the entry to be processed within the configuration memory (Rodgers et al., Abstract, column 16, line 50-column 17, line 3, The register which holds the pointer to the jump table.).

31. Referring to claim 9, Casselman in combination with Rodgers et al. and Schrofer have taught the method according to Claim 1, characterized in that the PLU contains an address register which points at the address (number, coordinates, etc.) of the cell which has triggered an event (Rodgers et al., Abstract, column 16, line 50-column 17, line 3, The address of the cell which triggered an event must inherently be stored in a register.).

32. Referring to claim 10, Casselman in combination with Rodgers et al. and Schrofer have taught the method according to Claim 1, characterized in that the PLU contains a data register containing configuration data which is transmitted to the cell in a reconfiguration (Casselman,

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Figure 4, The register where the configuration bit files that are produced by the mother FPGA are stored.).

33. Referring to claim 11, Casselman in combination with Rodgers et al. and Schrofer have taught the method according to claim 1, characterized in that the PLU contains a dispatch register which contains the address of the entry in the jump table calculated from the cell address (Rodgers et al., Abstract, column 16, line 50-column 17, line 3, The address of the entry must inherently be stored in a register.).

***Conclusion***

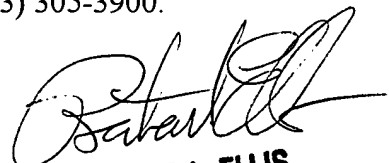
34. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L Meonske whose telephone number is (703) 305-3993.

The examiner can normally be reached on Monday-Friday, 8-4:30.

35. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie P Chan can be reached on (703) 305-9712. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

36. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

tlm  
July 17, 2003

  
RICHARD L. ELLIS  
PRIMARY EXAMINER